Virtual Plating: Emerging Technology Unravels the Mysteries of Electrodeposition

by **ROGER W. MOUTON**

With the advent of modern, sophisticated computer hardware, capable of rapidly crunching large amounts of numbers, formulae and information, it has become possible to generate complex manufacturing models and realistic scenarios that are occasionally termed "virtual."

Since the early 1970s, virtual worlds have been created by mathematical models and computer programs. Most of us are familiar with the term "virtual reality." It was born in the entertainment industry. Some may think that to understand and see into the virtual world, it is essential to use HMDs (head-mounted devices). It is not. A simple desktop computer will do.

Virtual reality (VR) is currently used to explore and manipulate real and experimental data in ways that were not before possible. Medical therapists can use VR to treat people who are afraid of heights. Muscular dystrophy patients can learn to use a wheelchair through virtual reality. Engineers using VR can be more effective in finding optimum manufacturing solutions needed to meet existing and future electronic design and manufacturing challenges.

Virtual, as applied to manufacturing technology in the printed circuit industry, was discussed in a previous volume of *The Board Authority*; Vol. 2, Number 4, "Virtual Prototyping." The modeling of most any board manufacturing process is seen as possible.

VIRTUAL PLATING

Enter "Virtual Plating." Electroplating of complex substrates is difficult because the substrates don't have cathodic potentials that exactly match the anodic fixtures in the electroplating vessel. The result is that plating deposits are of non-uniform thickness.

The reasons for this non-uniformity are many. For one, the anodic substrates are generally "fixed" and contained in a rectangular or square plating vessel with a flat bottom. Virtual plating is an excellent way to better understand anode/cathode relationships and take steps to optimize the plating set-up to achieve uniform deposit thicknesses.

The cathodic substrates (printed circuit boards) have varying sizes and surface features. It's fortunate that the board is at least flat because it makes fixturing relatively straightforward. It also makes conveyorizing of the plating process possible.

The numerous surface and PTH features, e.g., traces, vias, holes and pads, are the problem. They present such varying electrode potentials that inherent plating thickness non-uniformities become detrimental to productivity, costs, and quality. The most common electroplating thickness specification for acid copper plating deposits is 1.0 mils. Because of the basic substrate shape (generally flat) and the varying configurations of circuit features on the surface and in the holes of the board, it is very difficult to achieve overall plating thickness uniformity.

If panel plating is the chosen method for copper deposition, non-uniform plating deposits frequently cause etching difficulties and etching must then function only in a limited or narrow process window. If the pattern plating process is employed, plating predictability and uniform deposits also become extremely hard to achieve for reasons as numerous as there are different designs.

Frequently, a plated circuit board with a minimum acid copper thickness specification of 1.0 mils measures well in excess of 2.0 mils on different parts on the board.

Mils Cu	Design A	Design B	Design C
IT	2.5	2.8	3.0
IP	2.8	2.0	2.6
CT	1.8	1.5	1.0
BV	0.8	1.0	1.0
PTH	1.0	0.75	1.0

IT = Isolated Trace(s); IP = Isolated Pad(s); CT = Average Circuit Trace; BV = Blind Vias; PTH = Plated Through Holes

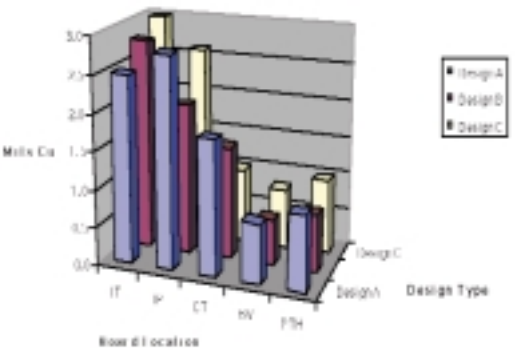

Figure 1a (top), 1b (bottom). Typical Acid Copper Pattern Plating Performance.

Figures 1a and 1b illustrate typical acid copper pattern plating performance on three different multilayer circuit board designs, i.e., with varying surface and hole features and varying plating thickness measurements. In this example, PTH aspect ratios are all in excess of 10:1, and blind via aspect ratios do not exceed 1.5:1 (5-mil holes/7.5-mils deep).

It is an accepted fact of circuit board plating life that non-uniform deposits (overplating) occur. Plating vessel geometry, and anodic/cathodic features, including fixturing, become critical plating issues that can also manifest themselves in underplating. Underplating (below the specified thickness of 1.0 mils Cu) in holes, especially blind via holes, can frustratingly be a common result while overplating (exceeding specified thickness) is

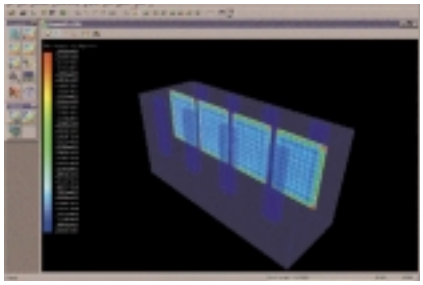

Figure 2. Parallel Anode Set-Up, Using Rectangular Anode Baskets.

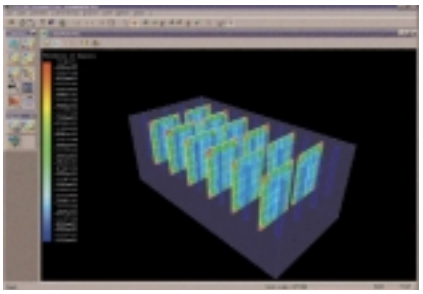

Figure 3. Perpendicular Anode Set-Up, Using Round Baskets.

present on different parts of the same board. Industry response to this is usually to plate at lower current densities and for longer times.

How does virtual plating relate to this and how can it assist the board fab plating engineer? Three dimensional modeling and simulation is one of the answers.

3D MODELING AND SIMULATION

Figures 2 and 3 represent 3D modeling of simple acid copper panel plating on multilayer substrates in two different plating vessel/fixturing set-ups.

The simulated plating tests were performed at 15 a.s.f. for 1.5 hours. Figure 2 represents a parallel anode set-up using rectangular anode baskets while Figure 3 represents a perpendicular anode set-up using round baskets, both plating set-ups being in the same plating department.

The results of this 3D modeling and simulation, virtual plating, give clear direction to the plating engineer by predicting excessive thickness build-up on identical boards using two possible scenarios where the boards are plated at the same current density and for the same time.

An advantage of virtual plating as described is that a predicted deposit thickness can be displayed using color variations. These variations translate to plating thickness values. This is typical of modern boundary element and finite analytical methods. A particularly useful feature of virtual plating using this 3D modeling is that by clicking on a specific plated area with a mouse pointer, it's possible to "measure" the plated thickness at the selected point on the substrate.

The modeling of pattern plating on a board surface with varying surface features is depicted in Figure 4.

The electrode potentials of this complex multilayer board were simplified and analyzed using the board's design features. The board was shielded and plated in simulation. The simple shield is visible in the graphic as a small square border to protect overplating of the edges, especially the corners. The virtual plating results reveal potential "hot" spots or areas of overplating that might be troublesome on the board surface.

While this article doesn't specifically address the uniformity of plating in through-holes, it can be quickly deduced that if surface feature plating uniformity is achieved, through-hole plating performance will also necessarily be better. The most important factors affecting through-hole plating performance relate more to the volume of solution movement through the hole than to the actual current density in the hole.

If the current density is spread uniformly across the surface of the board, then all holes on that board, both blind and PTH holes, have a better than average chance of plating to the minimum thickness specification with a minimum of variation. In short, all the holes will be experiencing the same current density.

TRADE OFFS

When it comes to electroplating of circuit boards, there are many design and manufacturing trade-offs. If it's possible to know and/or predict the electroplating characteristics of a particular size or design of board, then it's possible to mediate those characteristics using a specific or ideal plating set-up using 3D modeling in virtual plating.

Figure 5 represents a simple anode/cathode model of parallel electrodes and the plating current flux lines that flow between them. It has been demonstrated that the scientific generation of flux line maps is possible. Therefore, knowing the size, shape, and orientation of parallel electrodes makes the job of virtual plating easier, and allows for more effective engineering of the plating set-up.

DESIGN FILES AND VIRTUAL PLATING

Circuit board design files contain significant amounts of information, e.g., the surface area of exposed platable area on each side of the board and, more important, the location(s) of that platable area. At present, that information is seldom used for plating set-up except to set current density levels for each side of the board and to understand exposed platable area in the holes.

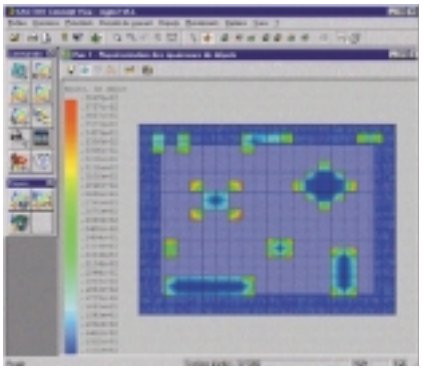

Figure 4. Modeling of Pattern Plating on a Board Surface.

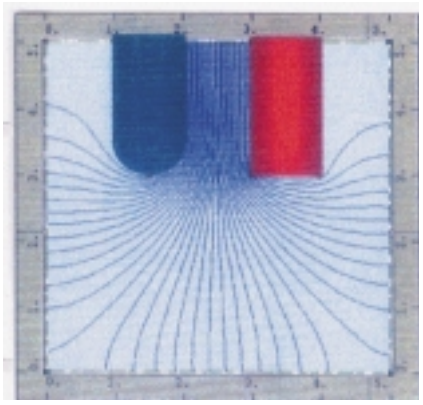

Figure 5. Flux Line Current Map.

Whether panel or pattern plating, it's commonly accepted that plating thickness nonuniformities will result. Knowing and using the available information, and using virtual plating technology in 3D modeling and plating simulation, can give important direction to design, fabrication, and the plating fixturing needed for a particular substrate.

Figure 6 represents a simple plating shield "grid" created from circuit board design files. The shield can be easily fabricated from any non-conductive, thin plastic material and affixed either to the plating rack or directly to the board through tooling holes.

Each quadrant in the grid is set up to allow specific densities of current to flow to corresponding areas of the board. The grid components can be perforated by drilling, routing, punching, or scoring to allow plating current flux lines to preferentially flow to desired areas on the board and to shield specific areas that would otherwise build excess deposit thicknesses.

Figure 7 depicts the relative density of the individual grid patterns in the shield. If, instead of slots, holes were drilled on the same centers across the face of the shield, then varying the hole sizes from small to

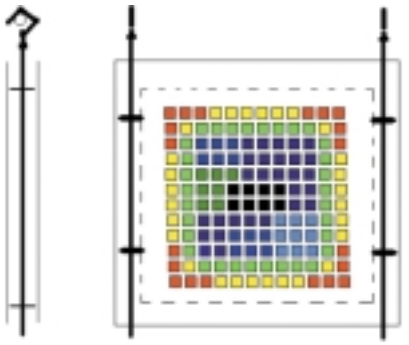

Figure 6. Simple Plating Shield Grid.

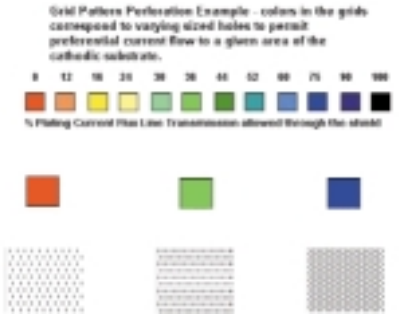

Figure 7 Relative Density of the Individual Patterns.

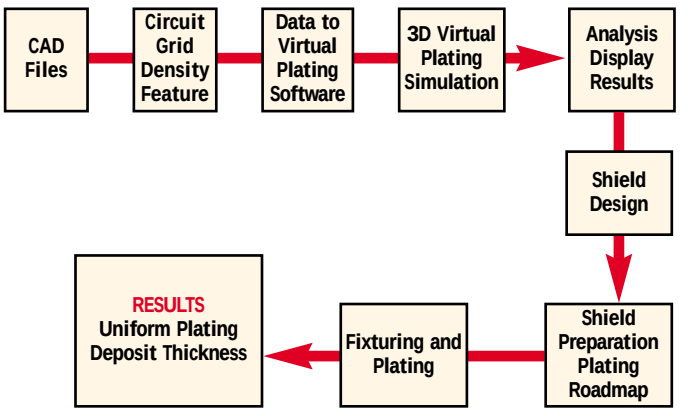

Figure 8. Manufacturing Steps.

large in the individual grids would accomplish the same objective.

The manufacturing steps in the modernized plating scenario as described might look like those in Figure 8.

There's no question that it would be a luxury to have a plating "roadmap" for each and every board that arrives in the plating department, regardless of its size or the complexity of its design.

Plating thickness uniformity improvement is, of course, relative. I know several board fab shops that would be ecstatic if their copper overplating didn't exceed 2.0 mils. Thus, the degree of plating performance desired or required determines the manufacturing actions taken to achieve them. Interestingly, there are other board fab problems that closely relate to plating but aren't always given consideration as such. Resist strip scrap loss is huge in some shops, and most of the time it's because of overplated traces. Butyl is once again being used as a band-aid for this process.

BENEFITS

Virtual plating offers the engineer a fast, simple and accurate means of experimenting with a "what if" plating scenario in ongoing efforts to improve plating performance. One of the reasons industry management talks about plating as "black magic" is that it's mysteries are many and difficult to figure out. Trial-and-error plating with all kinds of "what ifs" would eventually find improvements, given the law of averages, but trial-and-error plating experimentation in the manufacturing environment is costly, time consuming, and generally not practiced. Virtual plating changes all that.

Obvious benefits of plating improvement are:

- material cost reductions
- plating cycle time improvement
- quality improvement

It's important that if virtual plating using 3D modeling is learned and practiced in the printed circuit industry, we can begin to look for new heights to scale in electronic interconnect manufacturing. Virtual plating that turns into plating reality improvement is vital to the success of worldwide printed circuit manufacturing technology.

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